

FIG. 2 (Related Art)

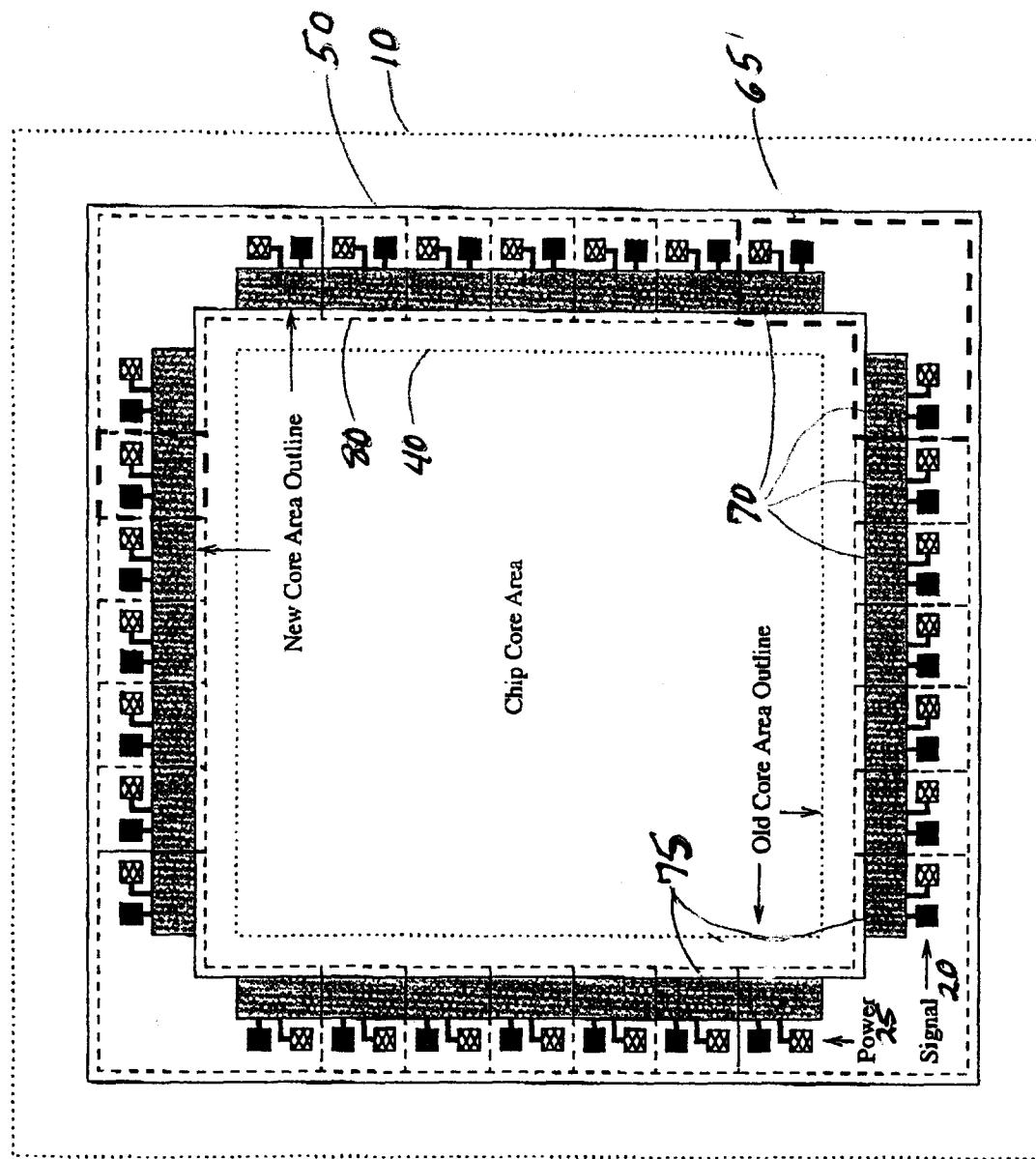


FIG. 3 (Related Art)

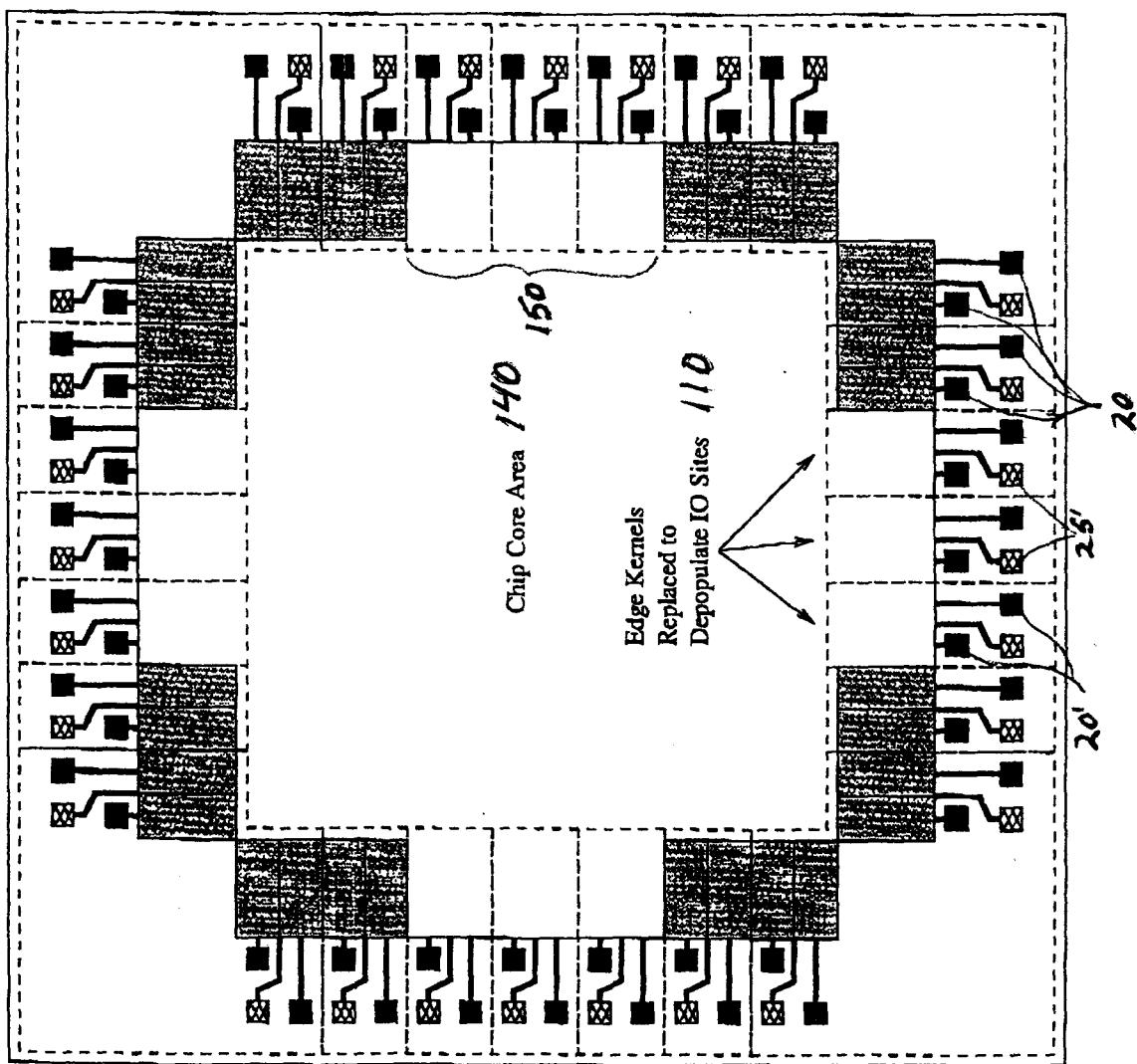


FIG. 4

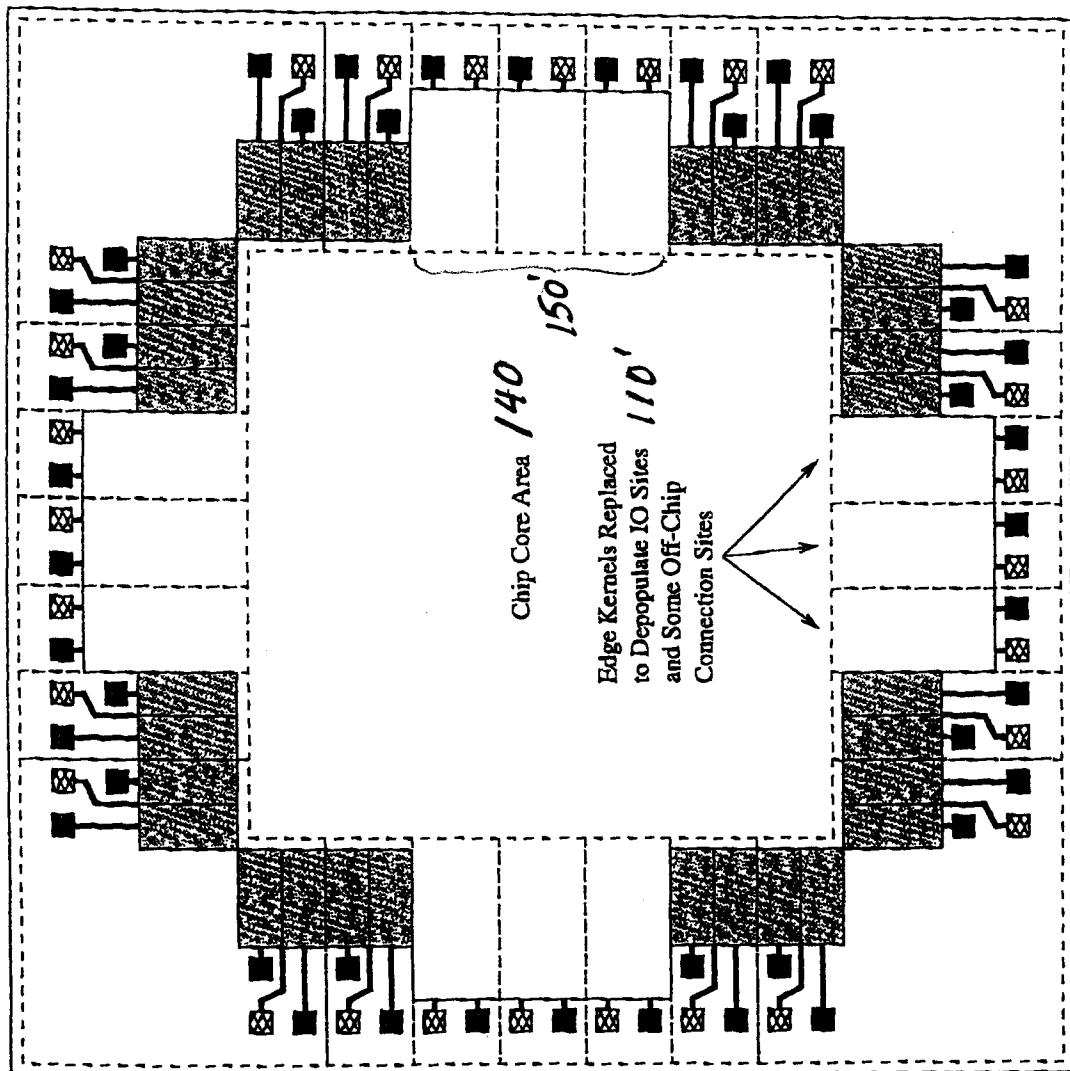


FIG 5

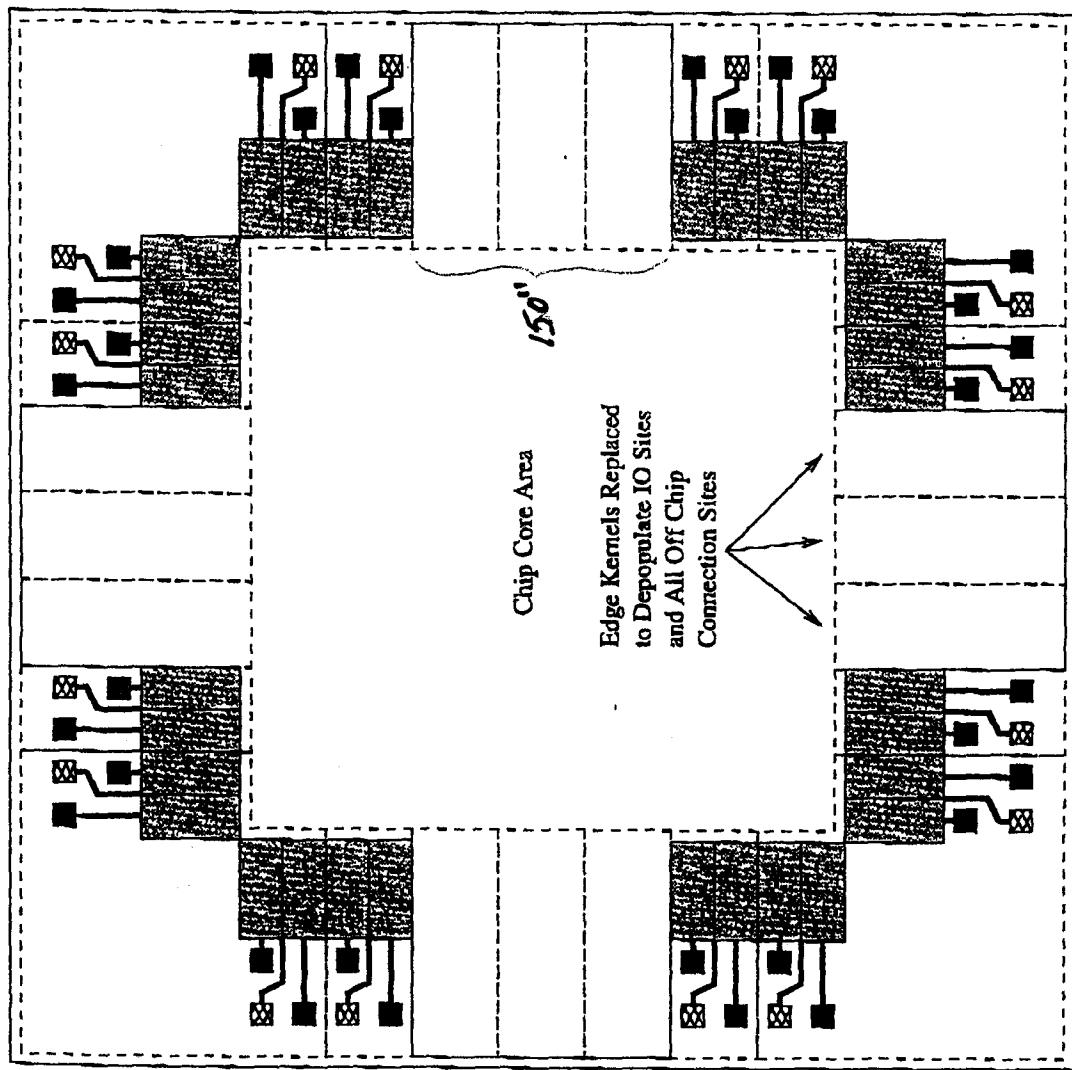


FIG. 5A

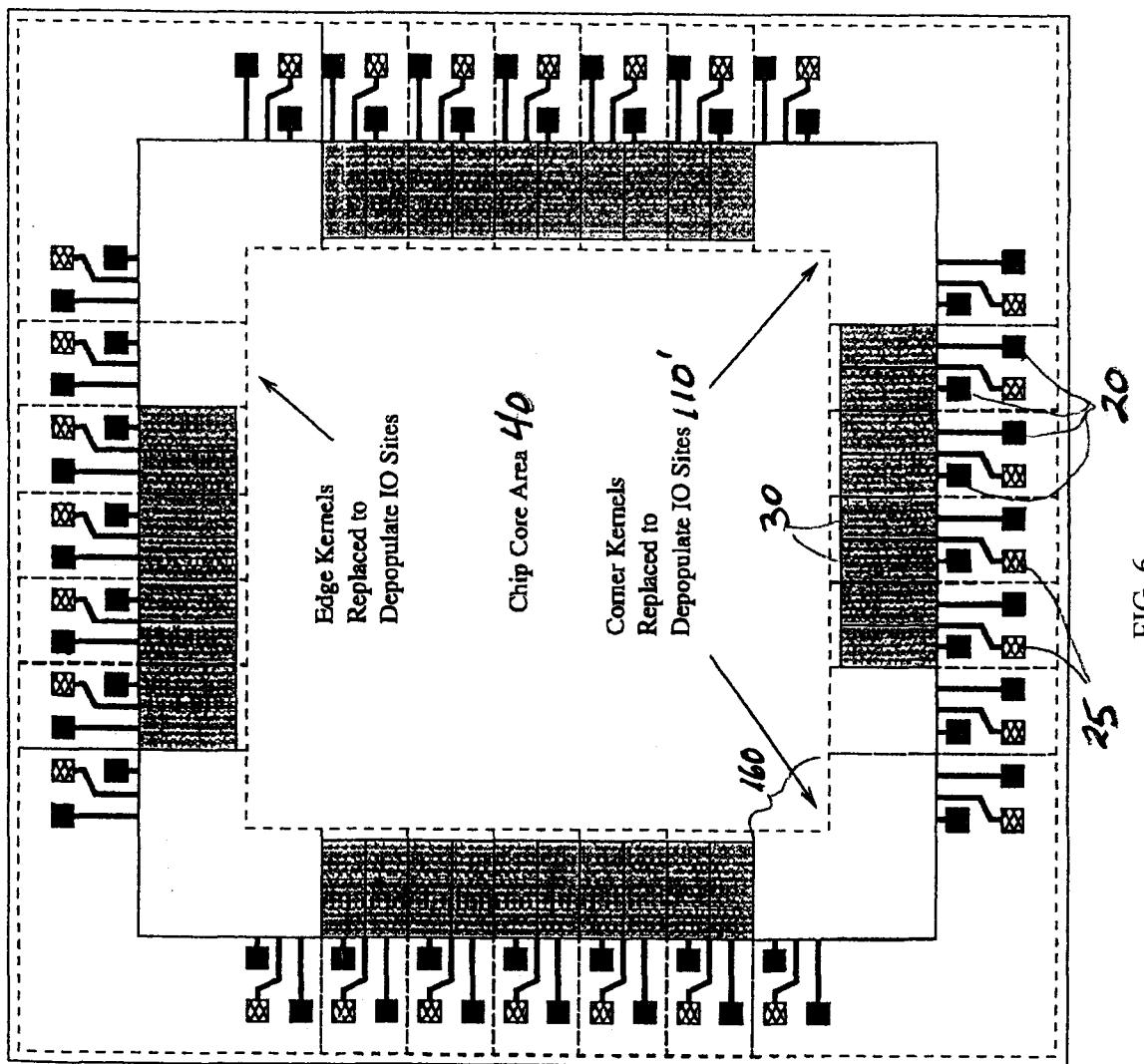


FIG. 6

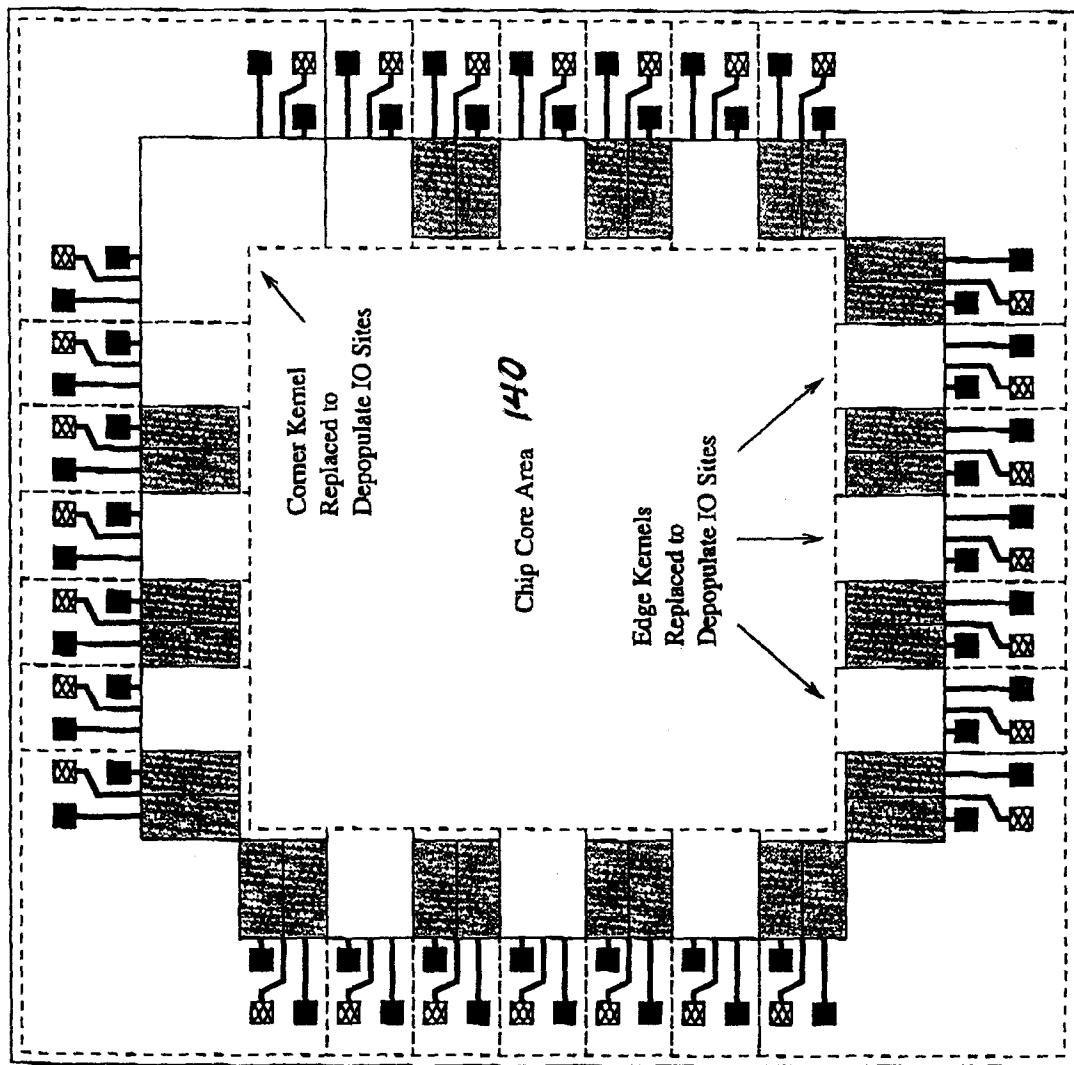


FIG. 7

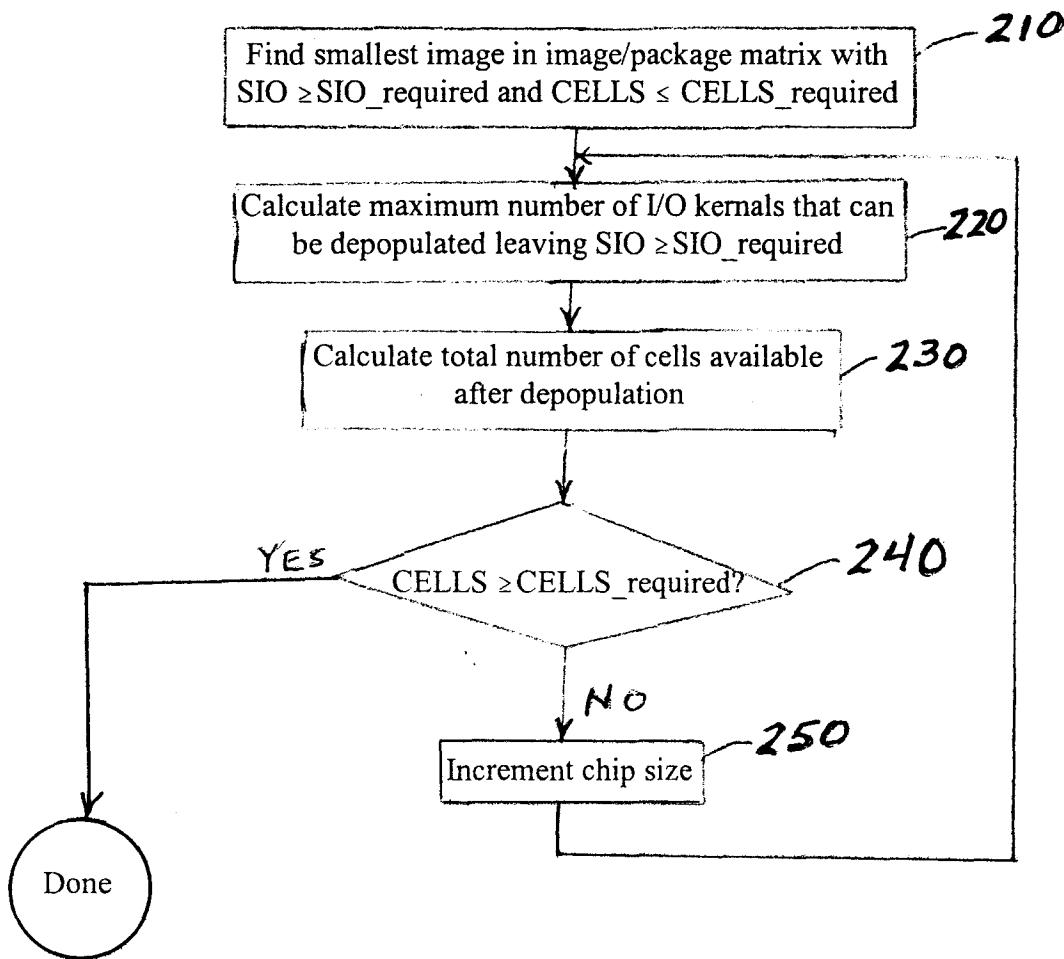


FIG. 8

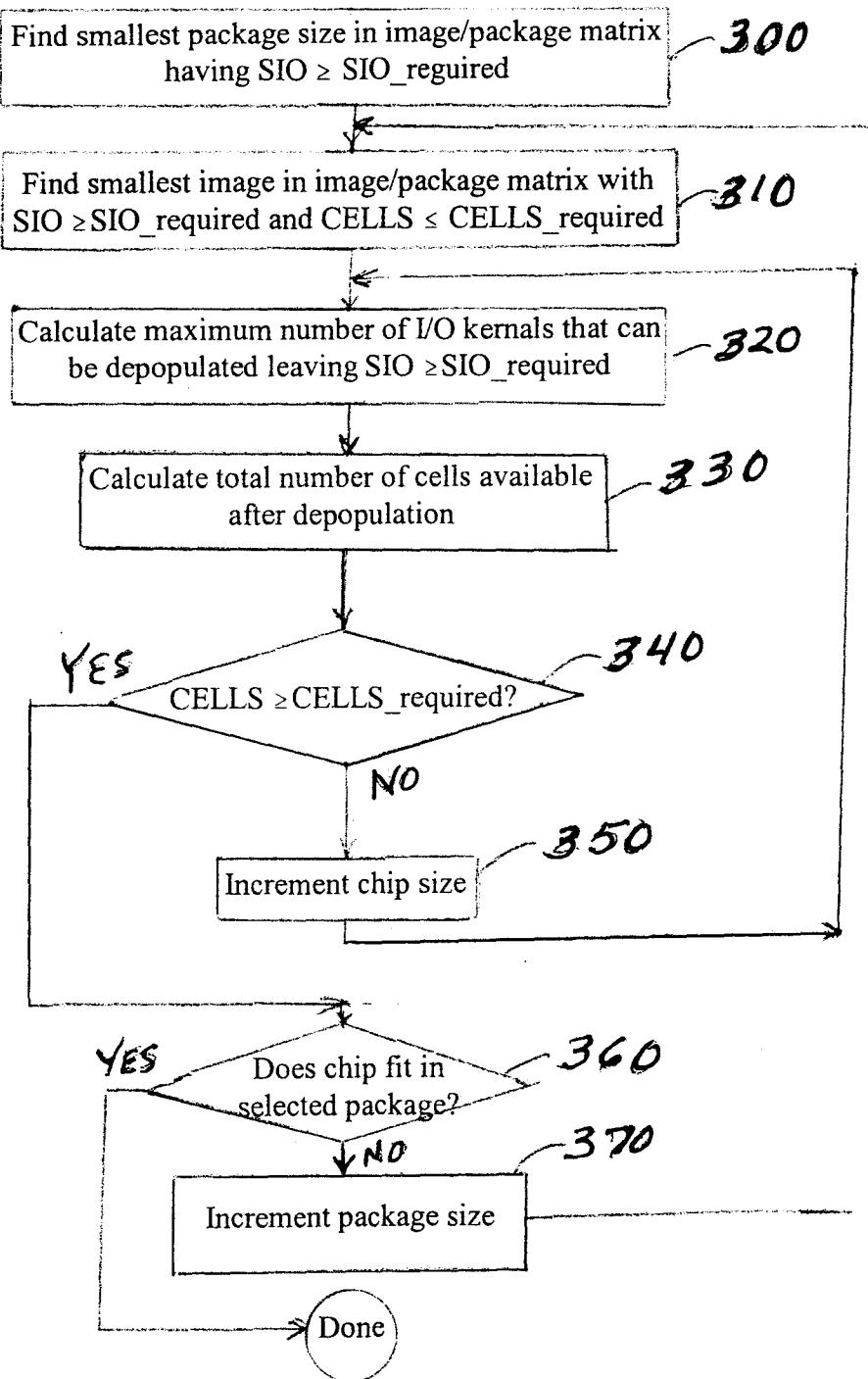


FIG. 9

Chip Image	4.85 mm x 4.85 mm	5.58 mm x 5.58 mm	6.30 mm x 6.30 mm
Core Cell Area (dimensions)	3.89 mm x 3.89 mm	4.62 mm x 4.62 mm	5.34 mm x 5.34 mm
Core Cell Area	15.13 mm <sup>2</sup>	21.34 mm <sup>2</sup>	28.52 mm <sup>2</sup>
Total Usable IO cell sites	352	416	480
# of edge kernel (per side)	8	10	12
# of corner kernel (per corner)	1	1	1

Usable IO Sites per Edge Kernel	8
Core Area Recovered by replacing an edge kernel	0.36 mm <sup>2</sup>
Usable IO Sites per Corner Kernel	24
Core Area Recovered by replacing a corner kernel	1.0 mm <sup>2</sup>

FIG. 10